

**ABSTRACT**

A flash memory device having a reduced source resistance and a fabrication method thereof are disclosed. An example flash memory includes a cell region including a gate, a source line, a drain contact, and a cell trench area for device isolation on a silicon substrate. The example flash memory also includes a peripheral region positioned around the cell region and including a subsidiary circuit and a peripheral trench area for device isolation on the silicon substrate, wherein the cell trench area of the cell region is shallower than the peripheral trench area of the peripheral region.